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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,706	07/24/2006	Takefumi Nishimuta	5000-5291	9357

27123 7590 11/16/2007
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EXAMINER	
BELOUSOV, ALEXANDER	
ART UNIT	**PAPER NUMBER**
2811	

NOTIFICATION DATE	DELIVERY MODE
11/16/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/560,706	NISHIMUTA ET AL.	
	Examiner	Art Unit	
	Alexander Belousov	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *14-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☒ Claim(s) *1-3,5,7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE GURLEY
SUPERVISORY PATENT EXAMINER
AU 2811, TC 2800

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/13/2005 & 04/03/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election **without traverse** of claims 1-13 in the reply filed on 10/03/2007 is acknowledged. **Claims 14-19** are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected group. Election was made **without** traverse in the reply filed on 10/03/2007.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 12/13/2005 & 04/03/2006. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

Claim 1 recites the limitation "a single conductivity type diffusion **region** formed in the projecting part facing each of said at least two different crystal planes constituting the surface of the projecting part and **individually formed on both sides** of the gate electrodes". There is insufficient antecedent basis for the multiple regions, since only one region is recited above.

Claim 1 recites the limitation "a single conductivity type diffusion region formed in the projecting part facing each of said at least two different crystal planes constituting the surface of the projecting part and individually formed on both sides of the **gate electrodes**". There is insufficient antecedent basis for multiple gate electrodes, since only one gate electrode is recited above.

Claim 2 recites the limitation "single conductivity diffusion **regions**". There is insufficient antecedent basis for multiple diffusion regions, since only one diffusion region is recited above.

Claim 3 is objected to because of the following informalities: the preamble reads "MIS transistor according to claim 1 **or** wherein". The "or" appears to be a typo. Appropriate correction is required.

Claim 5 recites the limitation "a single conductivity type diffusion region formed in the projecting part facing each of said at least two different crystal planes constituting the surface of the projecting part and individually formed on both sides of the **gate electrodes**". There is insufficient antecedent basis for multiple gate electrodes, since only one gate electrode is recited above.

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 7 & 8 are objected to under 37 CFR 1.75 as being a substantial duplicate of **claim 6**. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim

to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claim 1-13** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claim limitations of "semiconductor substrate comprising a projecting part of which the surfaces are at least two different crystal planes on a principal plane", as recited in **claim 1**, are unclear as to which element is formed on a principal plane. Also, the claim limitations of "a single conductivity type diffusion **region** formed in the projecting part facing each of said at least two different crystal planes constituting the surface of the projecting part and **individually formed on both sides** of the gate electrodes", as recited in claim 1, are unclear as to which **elements** are individually formed on both sides of the gate electrodes.

The claim limitations of "semiconductor substrate comprising a projecting part of which the surfaces are at least two different crystal planes on a principal plane", as recited in **claim 5**, are unclear as to which element is formed on a principal plane. Also, the claim limitations of "a single conductivity type diffusion **region** formed in the projecting part facing each of said at least two different crystal planes constituting the principal plane and surface of the projecting part and **individually formed on both sides** of the gate electrodes", as recited in claim 5, are unclear as to which **elements** are individually formed on both sides of the gate electrodes.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1-13** are rejected under 35 U.S.C. 102(b) as being anticipated by (US-20030102497) by Fried et al.

Regarding claim 1, Fried discloses in FIG. 7A-7B and related text MIS transistor (paragraph 2; FINFET C**MOS**), formed on a semiconductor substrate (206), comprising: a semiconductor substrate (206) comprising a projecting part of which the surfaces are at least two different crystal planes on a principal plane (Abstract; also, FIG. 7B; the surface of the 206 that is next to 208 and one of the surfaces of 206 that is next to 210 are the two planes); a gate insulator (208 & 210) for covering at least a part of each of said at least two different crystal planes constituting the surface of the projecting part; a gate electrode (212) comprised by the gate insulator so as to be electrically insulated from the semiconductor substrate, and comprised on each of said at least two different crystal planes constituting the surface of the projecting part; and a single conductivity type diffusion region formed in the projecting part (paragraph 57; "The S/D regions .. comprising the fin bodies") facing each of said at least two different crystal planes constituting the surface of the projecting part and individually formed on both sides of the gate electrodes (see FIG. 7a; they are on both sides of 214).

Regarding claim 2, Fried discloses in FIG. 7A-7B and related text the channel width of a channel formed along with the gate insulator between the single conductivity diffusion regions

individually formed on both sides of the gate electrodes is indicated by summation of the channel widths of each channel generated along said at least two different crystal planes (see FIG. 7B).

Regarding claim 3, Fried discloses in FIG. 7A-7B and related text the gate insulator covers said at least a part of each of said at least two different crystal planes, which configure the surface of the projecting part, so that said at least two different crystal planes are continuously covered (inherent: otherwise gate would short to substrate and the device would not be operational).

Regarding claim 4, Fried discloses in FIG. 7A-7B and related text the gate insulator covers said at least a part of each of said at least two different crystal planes which configure the surface of the projecting part so that said at least two different crystal planes are continuously covered (see FIG. 7B; also inherent: otherwise gate would short to substrate and the device would not be operational).

Regarding claim 5, Fried discloses in FIG. 7A-7B and related text MIS transistor (Abstract: FinFET), formed on a semiconductor substrate (206), comprising: a semiconductor substrate (206) comprising a projecting part of which the surfaces are at least two different crystal planes on a principal plane (Abstract; also, FIG. 7B; the surface of the 206 that is next to 208 and one of the surfaces of 206 that is next to 210 are the two planes); a gate insulator (208 & 210) for covering at least a part of each of said at least two different crystal planes constituting the principal plane (top surface of 206; next to 208) and the surface (one of the side surfaces of 206; next to 210) of the projecting part; a gate electrode (212) comprised by the gate insulator so as to be electrically insulated from the semiconductor substrate, and comprised on each of said at least two different crystal planes constituting the principal plane and the surface of the projecting

part; and a single conductivity type diffusion region (paragraph 5: source/drain regions) formed in the projecting part facing each of said at least two different crystal planes constituting the principal plane and surface of the projecting part and individually formed on both sides of the gate electrodes.

Regarding claim 6, Fried discloses in FIG. 7A-7B and related text the gate insulator covers at least a part of each of said at least two different crystal planes, which configure the principal plane and the surface of the projecting part, so that the principal plane and said at least two different crystal planes are continuously covered (inherent: otherwise gate would short to substrate and the device would not be operational).

Regarding claim 7, Fried discloses in FIG. 7A-7B and related text the gate insulator covers at least a part of each of said at least two different crystal planes, which configure the principal plane and the surface of the projecting part, so that the principal plane and said at least two different crystal planes are continuously covered (inherent: otherwise gate would short to substrate and the device would not be operational).

Regarding claim 8, Fried discloses in FIG. 7A-7B and related text the gate insulator covers at least a part of each of said at least two different crystal planes, which configure the principal plane and the surface of the projecting part, so that the principal plane and said at least two different crystal planes are continuously covered (inherent: otherwise gate would short to substrate and the device would not be operational).

Regarding claim 9, Fried discloses in FIG. 7A-7B and related text being a signal transistor (inherent: transistors can be "on" or "off", hence at least two different signals).

Regarding claim 10, Fried discloses in FIG. 7A-7B and related text being a signal transistor (inherent: transistors can be "on" or "off", hence at least two different signals).

Regarding claim 11, Fried discloses in FIG. 7A-7B and related text the semiconductor substrate is a silicon substrate (paragraph 44: "**any** semiconductor material") and the hydrogen content at an interface of the silicon substrate and the gate insulator is 10.sup.11/cm.sup.2 or less in units of surface density (Fried does not disclose **any** usage of hydrogen, hence the hydrogen content is "zero").

Regarding the process limitations recited in claim 11 ("the gate insulator **is formed by** exposing the surface of the silicon substrate to a plasma of a prescribed inert gas so as to remove hydrogen"), these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claim 12, Fried discloses in FIG. 7A-7B and related text the semiconductor substrate is a silicon substrate (paragraph 44: "**any** semiconductor material"), and the hydrogen

content at an interface of the silicon substrate and the gate insulator is 10.sup.11/cm.sup.2 or less in units of surface density.

Regarding the process limitations recited in claim 11 ("and the gate insulator **is formed by** exposing the surface of the silicon substrate to a plasma of a prescribed inert gas so as to remove hydrogen"), these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claim 13, Fried discloses in FIG. 7A-7B and related text the semiconductor substrate is a silicon substrate (paragraph 44: "any semiconductor material") and the principal plane and said at least two different crystal planes are any two different crystal planes from the (100) plane, the (110) plane and the (111) plane (paragraph 40).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References A & B are cited as being related to hydrogenation of surface.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Belousov whose telephone number is 571-270-3209. The examiner can normally be reached on Monday - Thursday 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Alexander Belousov
November 5, 2007

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